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UTILITY PATENT APPLICATION TRANSMITTAL

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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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1. [X] Fee Transmittal Form
2. [X] Specification, Claims & Abstract ..... [Total Pages: 30]
3. [X] Drawing(s) *(35 USC 113)* ..... [Total Sheets: 10]
4. [X] Oath or Declaration ..... [Total Pages: 3]
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8. [X] Assignment Papers (cover sheet & document(s))
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10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
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18. CORRESPONDENCE ADDRESS

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SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT I, Yoshifusa Togawa, a citizen of Japan residing at Kawasaki-shi, Kanagawa, Japan have invented certain new and useful improvements in

INFORMATION PROCESSING APPARATUS, POWER CONTROL METHOD AND RECORDING MEDIUM

of which the following is a specification : -

TITLE OF THE INVENTION

INFORMATION PROCESSING APPARATUS, POWER CONTROL METHOD AND RECORDING MEDIUM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to information processing apparatuses, power control methods and recording media, and more particularly to an information processing apparatus which drives a plurality of processing units according to different types of files, a power control method therefor and a recording medium used therewith.

In recent years, information processing apparatuses have become small sized and portable because they can operate using batteries. Maximum reduction of dissipation power is needed for these apparatuses. On the other hand, multimedia devices have progressed, such that data which is processed in the information processing apparatuses now consist of a plurality of types of data such as moving pictures, sound and still pictures. It is necessary to activate a graphics board to display the moving pictures and still pictures and to activate a sound board to play back the sound data. However, only the sound board needs to be activated when the sound data is played back, but the moving pictures and still pictures are not displayed. In this case, if both the sound board and the graphics board are activated together, the power efficiency degrades because power which is supplied to the graphics board is wasted. Accordingly, it is desired to raise the power efficiency.

2. Description of the Related Art

Conventionally, personal computers use power save functions which become active if an

access to the personal computers does not occur or each of processing units spontaneously moves into a suspend mode. Japanese Laid-Open Patent Application No.57-104992, Japanese Laid-Open Patent Application No.62-34218, Japanese Laid-Open Patent Application No.4-364266, Japanese Laid-Open Patent Application No.8-307783 and Japanese Laid-Open Patent Application No.9-163043 disclose examples of methods to achieve a high power efficiency for electrical apparatuses.

Japanese Laid-Open Patent Application No.57-104992 discloses a power save control method. In the method, a first mode or a second mode is detected. When the second mode is detected, power which is supplied in the first mode is shut down. Therefore, the first mode becomes inactive when the second mode is active.

Japanese Laid-Open Patent Application No.62-34218 discloses an electrical apparatus of which operators can decide whether to execute a power save operation.

Japanese Laid-Open Patent Application No.4-364266 discloses a power save apparatus for a sound circuit to shut down the sound circuit according to a result of detection of whether a CD is a CD-ROM or a musical CD based on TOC (Table of Contents) information.

Japanese Laid-Open Patent Application No.8-307783 discloses a television apparatus which is equipped with a CD player. The television apparatus detects whether a CD is in place in the CD player. If the CD is in place in the CD player, the television apparatus detects a type of the CD. Then, the television apparatus controls the CD player according to the presence of the CD in it and drives necessary circuits according to the type of the CD.

Japanese Laid-Open Patent Application

No.9-163043 discloses a copy system, to which sub-controllers for expansion may or may not be connected, which copy system enables an optimum power save control. However, the copy system does not execute the power save control if the sub-controllers for expansion are not connected.

The method disclosed in Japanese Laid-Open Patent Application No.57-104992 only executes the power save control according to the mode. Therefore, the method does not achieve a precise power save control according to a type of data or for each of the processing units.

In the method disclosed in Japanese Laid-Open Patent Application No.62-34218, each of the processing units which is not used must be manually shut down. As users don't usually shut down the processing units, power is not saved.

The apparatus disclosed in Japanese Laid-Open Patent Application No.4-364266 executes a power save control according to the TOC information of each medium when a CD-ROM is inserted and its TOC information is read. Therefore, it does not achieve the precise power save control.

The apparatus disclosed in Japanese Laid-Open Patent Application No.8-307783 controls circuits according to whether a CD is inserted in it and the type of CD when the CD is inserted. It does not execute the precise power save control according to information recorded on the CD or for each processing unit which is driven.

The copy system disclosed in Japanese Laid-Open Patent Application No.9-163043 only executes the power save control when the sub-controllers for expansion are connected. Therefore, it does not achieve the precise power save control according to the type of data or for each of the processing units.

SUMMARY OF THE INVENTION

It is a general object of the present invention to provide information processing apparatuses, power control methods and recording medium in which the above disadvantages are eliminated.

A more specific object of the present invention is to provide information processing apparatuses, power control methods and recording medium which achieve the precise power save control.

The above objects of the present invention are achieved by an apparatus which drives a plurality of driving units according to data to be processed. The information processing apparatus includes a detection unit which detects type of the data to be processed and a control unit which controls each of the plurality of driving units according to the type of the data to be processed.

The above objects of the present invention are achieved by an apparatus which drives a plurality of driving units according to data to be processed. The information processing apparatus includes a control unit which controls each of the plurality of driving units according to control data added to the data to be processed.

The above objects of the present invention are achieved by a method which controls power supplied to a plurality of driving units to be supplied with data to be processed. The power control method includes the steps of (a)detecting a type of the data to be processed and (b)controlling each of the plurality of driving units according to said type of the data to be processed.

The above objects of the present invention are achieved by a method which controls power supplied to a plurality of driving units to be

supplied with data to be processed. The power control method includes a step for controlling each of the plurality of driving units according to control data added to the data to be processed.

The above objects of the present invention are also achieved by a computer readable recording medium from which a program can be read by a computer that drives a plurality of driving units according to data to be processed. The computer readable recording medium includes the program which has a detection procedure for detecting a type of the data to be processed and a control procedure for controlling each of the plurality of driving units according to the type of the data to be processed.

The above objects of the present invention are also achieved by a computer readable recording medium from which a program can be read by a computer that drives a plurality of driving units according to data to be processed. The computer readable recording medium includes the program which has a control procedure for controlling each of the plurality of driving units according to control data added to the data to be processed.

The above objects of the present invention are also achieved by a computer readable recording medium which includes data that has driving data to be supplied to driving units and control data used to control other driving units.

According to this invention, the types of the data are detected and if the data can not be processed by the driving units, the driving units can be stopped. Consequently, the driving units which are not used are automatically stopped, so that dissipation power can be reduced.

According to this invention, the types of the data are detected and if the data can not be processed by the driving units, the driving units

are not supplied with the power. Consequently, the driving units which are not used are automatically stopped, so that the dissipation power can be reduced.

Further, according to this invention, the driving units are controlled by the control data which are added to the data. Consequently, the driving units which are not used are automatically stopped, so that the dissipation power can be reduced.

According to this invention, the driving units are selected according to the control data used to control the driving units. The driving units which are not used are not supplied with the power. Consequently, the driving units which are not used are automatically stopped, so that the dissipation power can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features and advantages of the present invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram of a first embodiment of the present invention;

Fig. 2 is a block diagram of a hard disc drive controller according to the first embodiment of the present invention;

Fig. 3 is a block diagram of a floppy disc drive controller according to the first embodiment of the present invention;

Fig. 4 is a block diagram of a sound board controller according to the first embodiment of the present invention;

Fig. 5 is a block diagram of a graphics board controller according to the first embodiment

of the present invention;

Fig. 6 is a flowchart for registering a power save mode according to the first embodiment of the present invention;

Fig. 7 is a data structure of a power save mode table according to the first embodiment of the present invention;

Fig. 8 is a flowchart of a power save control in a CPU according to the first embodiment of the present invention;

Fig. 9 is another example of a data structure of a register for the power save mode table according to the first embodiment of the present invention; and

Fig. 10 is a flowchart of a power save control in the CPU according to a second embodiment of the present invention;

Fig. 11 is a structure of data processed by the CPU according to the second embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig.1 is a block diagram of a first embodiment of the present invention. An information processing apparatus 100 of this embodiment is mainly made up of a CPU 101, a memory 102, a ROM 103, a hard disc drive 104, a hard disc drive controller 105, a floppy disc drive 106, a floppy disc drive controller 107, a CD-ROM drive 108, a sound board 109, a speaker 110, a sound board controller 111, a graphics board 112, a display device 113, a graphics board controller 114 and a bus 115.

The CPU 101 processes data by desired programs. The memory 102 stores the program and the data. The ROM 103 stores an OS to boot up the information processing apparatus 100.

The hard disc drive 104 mainly include a

main body of the hard disc drive 116 and a hard disc drive control board 117. The main body of the hard disc drive 116 has hard discs 118 in it and magnetically stores and retrieves the data on the hard discs. The hard disc drive control board 117 controls the main body of the hard disc drive 116 in response to commands from the bus 115.

The hard disc drive controller 105, which is connected between the hard disc drive 104 and the bus 115, controls the hard disc drive 104 in response to the data processed by the CPU 101.

The floppy disc drive 106 is mainly composed of a main body of the floppy disc drive 119 and a floppy disc drive control board 120. The main body of the floppy disc drive 119, into which a floppy disc 121 is inserted, magnetically stores and retrieves the data on the floppy discs. The floppy disc drive control board 120, which is connected between the main body of the floppy disc drive 119 and the floppy disc drive controller 107, controls the main body of the floppy disc drive 119 in response to the commands from the bus 115.

The floppy disc drive controller 107, which is connected between the floppy disc drive 106 and the bus 115, controls the floppy disc drive 106 in response to the data processed by the CPU 101.

The CD-ROM drive 108, into which a CD-ROM disc 122 is inserted, reads recorded data on the CD-ROM disc in response to the commands from the bus 115 and supplies the data to the bus 115.

The sound board 109 converts sound data into analog sound signals, amplifies them and supplies them to the speaker 110. The speaker 110 converts the analog sound signals into sounds.

The sound board controller 111, which is connected between the sound board 109 and the bus 115, controls the sound board 109 in response to the

data processed by the CPU 101.

The graphics board 112 converts the data from the bus 115 into signals which can be displayed on the display device 113, e.g., RGB signals, and supplies them to the display device 113. The display device 113 displays pictures according to the signals from the graphics board 112.

The graphics board controller 114, which is connected between the graphics board 112 and the bus 115, controls the graphics board 112 in response to the data processed by the CPU 101.

The CPU 101, the memory 102, the ROM 103, the hard disc drive 104 through the hard disc drive controller 105, the floppy disc drive 106 through the floppy disc drive controller 107, the sound board 109 through the sound board controller 111 and the graphics board 112 through the graphics board controller 114 are attached to the bus 115. The commands and the data are exchanged among these components through the bus 115.

Fig.2 shows a block diagram of the hard disc drive controller 105 according to the first embodiment of the present invention. The hard disc drive controller 105 mainly has a gate 123, an OR gate 124, switches 125,126, and a register 127.

The gate 123 is connected to the bus 115, a voltage source 130 and the hard disc drive control board 117. The voltage source 130 converts an input power source Vin into a voltage source for the CPU 101, the memory 102, and so on.

The gate 123 controls the status of connection among the bus 115, the voltage source 130 and the hard disc drive control board 117 based on an output signal of the OR gate 124.

The OR gate 124 receives a power on/off flag 128 and a suspend/resume flag 129 from the register 127 and outputs a logical add value. The

register 127 is connected to the CPU 101 and holds values in the power on/off flag 128 and the suspend/resume flag 129 in response to commands from the CPU 101.

The switch 125 is connected to the input power source Vin, a voltage source of the hard disc drive 131 and the switch 126. The voltage source of the hard disc drive 131 converts the input power source Vin into a voltage source for the hard disc drive 104. The switch 125 changes its state between on and off according to the power on/off flag 128 in the register 127 and controls supply of the input voltage Vin to both the voltage source of the hard disc drive 131 and the switch 126.

The switch 126 is connected to the switch 125 and the main body of the hard disc drive 116 and controls supply of the voltage Vin to motors in the main body of the hard disc drive 116. The switch 126 changes its state between on and off according to the suspend/resume flag 129 in the register 127 and controls supply of the input voltage Vin to the main body of the hard disc drive 116.

The CPU 101 detects a type of the data of a file with a method described later and writes the values to both the power on/off flag 128 and the suspend/resume flag 129 in the register 127 according to the detected type of the data of the file.

The hard disc drive controller 105 turns the switch 125 on when the power on/off flag 128 in the register 127 is "1"(one). When the switch 125 turns on, power is supplied to both the switch 126 and the voltage source of the hard disc drive 131. Then, if the switch 126 is on, power is supplied to the main body of the hard disc drive 116 and consequently a spindle motor is driven.

Then, if the switch 126 is on, the

data can be stored on or retrieved from the hard discs 118. When the power on/off flag 128 in the register 127 is "1"(one), the gate 123 turns on and power is supplied to the hard disc control board 117. As a result, the hard disc control board 117 is connected to the bus 115, so that commands from the bus 115 may be for processed.

If the power on/off flag 128 in the register 127 is "0"(zero), the hard disc drive controller 105 turns the switch 125 off and stops supplying the power to both the switch 126 and the voltage source of the hard disc drive 131.

If the power on/off flag 128 in the register 127 is "0"(zero), the gate 123 turns off, so that the hard disc drive control board 117 is disconnected from both the power and the bus 115.

As explained above, if the power on/off flag 128 in the register 127 is "0"(zero), the hard disc drive 104 completely stops.

The hard disc drive controller 105 turns the switch 126 on when the suspend/resume flag 129 in the register 127 is "1"(one). If the switch 125 is on, the power is supplied to the main body of the hard disc drive 116 and therefore the spindle motor is driven.

When the suspend/resume flag 129 in the register 127 is "1"(one), the gate 123 turns on and the power is supplied to the hard disc control board 117. As a result, the hard disc control board 117 is connected to the bus 115, so that commands from the bus 115 may be processed.

If the suspend/resume flag 129 in the register 127 is "0"(zero), the hard disc drive controller 105 turns the switch 126 off and stops the spindle motor in the main body of the hard disc drive 116.

If the suspend/resume flag 129 in the

register 127 is "0"(zero), the gate 123 turns off, so that the hard disc drive control board 117 is disconnected from the power and the bus 115.

As explained above, if the suspend/resume flag 129 in the register 127 is "0"(zero), while the power on/off flag 128 is "1"(one), the power is only supplied to the voltage source of the hard disc drive 131 in the hard disc drive 104. Therefore, only the circuits supplied with the power by the voltage source of the hard disc drive 131 are operational.

Next, the floppy disc drive controller 107 will be explained. Fig.3 shows a block diagram of the floppy disc drive controller according to the first embodiment of the present invention. The floppy disc drive controller 107 is mainly made up of a gate 132, an OR gate 133, switches 134,135, and a register 136.

The gate 132 is connected to the bus 115, the voltage source 130 and the floppy disc drive control board 120. The voltage source 130 converts the input power source Vin into a voltage source for the CPU 101, the memory 102, and so on.

The gate 132 controls the status of connection among the bus 115, the voltage source 130 and the floppy disc drive control board 120 based on an output signal of the OR gate 133.

The OR gate 133 receives a power on/off flag 137 and a suspend/resume flag 138 from the register 136 and outputs the logical add value. The register 136 is connected to the CPU 101 and holds values in the power on/off flag 137 and the suspend/resume flag 138 in response to commands from the CPU 101.

The switch 134 is connected to the input power source Vin, a voltage source of the floppy disc drive 139 and the switch 135. The voltage

source of the floppy disc drive 139 converts the input power source Vin into a voltage source for the floppy disc drive 106. The switch 134 changes its state between on and off according to the power on/off flag 137 in the register 136 and controls supply of the input voltage Vin to both the voltage source of the floppy disc drive 139 and the switch 135.

The switch 135 is connected to the switch 134 and the main body of the floppy disc drive 119 and controls supply of the voltage Vin to motors in the main body of the floppy disc drive 119. The switch 135 changes its state between on and off according to the suspend/resume flag 138 in the register 136 and controls supply of the input voltage Vin to the main body of the floppy disc drive 119.

The CPU 101 detects the type of the data of the file with the method described later and writes the values to both the power on/off flag 137 and the suspend/resume flag 138 in the register 136 according to the type of the data of the file.

The floppy disc drive controller 107 turns the switch 134 on when the power on/off flag 137 in the register 136 is "1"(one). When the switch 134 turns on, the power is supplied to both the switch 135 and the voltage source of the floppy disc drive 139. Then, if the switch 135 is on, the power is supplied to the main body of the floppy disc drive 119 and a spindle motor is driven.

Then, if the switch 135 is on, the data can be stored on and retrieved from the floppy discs 121. When the power on/off flag 137 in the register 136 is "1"(one), the gate 132 turns on and the power is supplied to the floppy disc control board 120. As a result, the floppy disc control board 120 is connected to the bus 115, so that commands from the bus 115 may be processed.

If the power on/off flag 137 in the register 136 is "0"(zero), the floppy disc drive controller 107 turns the switch 134 off and stops supplying the power to both the switch 135 and the voltage source of the floppy disc drive 139.

If the power on/off flag 137 in the register 136 is "0"(zero), the gate 132 turns off, so that the floppy disc drive control board 120 is disconnected from both the power and the bus 115.

As explained above, if the power on/off flag 137 in the register 136 is "0"(zero), the floppy disc drive 106 completely stops.

The floppy disc drive controller 107 turns the switch 135 on when the suspend/resume flag 138 in the register 136 is "1"(one). If both the switches 134 and 135 are on, the power is supplied to the main body of the floppy disc drive 119 and therefore the spindle motor is driven.

When the suspend/resume flag 138 in the register 136 is "1"(one), the gate 132 turns on and the power is supplied to the floppy disc control board 120. As a result, the floppy disc control board 120 is connected to the bus 115, so that commands from the bus 115 may be processed.

If the suspend/resume flag 138 in the register 136 is "0"(zero), the floppy disc drive controller 107 turns the switch 135 off and stops the spindle motor in the main body of the floppy disc drive 119.

If the suspend/resume flag 138 in the register 136 is "0"(zero), the gate 132 turns off, so that the floppy disc drive control board 120 is disconnected from the power and the bus 115.

As explained above, if the suspend/resume flag 138 in the register 136 is "0"(zero) while the power on/off flag 137 is "1"(one), the power is only supplied to the voltage source of the floppy disc

drive 139 in the floppy disc drive 106. Therefore, only the circuits supplied with the power by the voltage source of the floppy disc drive 139 are operational.

Next, the sound board controller 111 will be explained. Fig.4 shows a block diagram of the sound board controller according to the first embodiment of the present invention. The sound board controller 111 mainly includes a gate 140, an OR gate 141 and a register 142. The gate 140 is connected to the bus 115, the voltage source 130 and the sound board 109. The gate 140 controls the status of connection among the bus 115, the voltage source 130 and the sound board 109 based on an output signal of the OR gate 141.

The OR gate 141 receives a power on/off flag 143 and a suspend/resume flag 144 from the register 142 and outputs the logical add value. The register 142 is connected to the CPU 101 and holds values in the power on/off flag 143 and the suspend/resume flag 144 in response to commands from the CPU 101.

The CPU 101 detects the type of the data of the file with the method described later and writes the values to the power on/off flag 143 and the suspend/resume flag 144 in the register 142 according to the type of the data of the file.

The sound board controller 111 turns the gate 140 on when the power on/off flag 143 in the register 142 is "1"(one). If the gate 140 turns on, the sound board 109 is connected to both the voltage source 130 and the bus 115. The sound board 109 converts sound data into the analog sound signals and supplies them to the speaker 110. The speaker 110 converts analog sound signals into sounds.

If the power on/off flag 143 in the register 142 is "0"(zero), the gate 140 turns off,

so that the sound board 109 is disconnected from both the voltage source 130 and the bus 115. Therefore, the sound board 109 completely stops.

If the suspend/resume flag 144 in the register 142 is "1"(one), the sound board controller 111 turns on the gate 140, so that the sound board 109 is connected to both the voltage source 130 and the bus 115. Therefore, the sound board 109 is operational and drives the speaker 110 according to the data from the bus 115. The speaker 110 converts the analog sound signals into sounds.

If the suspend/resume flag 144 in the register 142 is "0"(zero), the gate 140 turns off, so that the sound board 109 is disconnected from both the voltage source 130 and the bus 115. Therefore, the sound board 109 completely stops.

Next, the graphics board controller 114 will be explained. Fig.5 shows a block diagram of the graphics board controller according to the first embodiment of the present invention.

The graphics board controller 114 includes a gate 145, an OR gate 146, a switch 147 and a register 148. The gate 145 is connected to the bus 115, the voltage source 130 and the graphics board 112. The gate 145 controls the status of connection among the bus 115, the voltage source 130 and the graphics board 112 based on an output signal of the OR gate 146.

The OR gate 146 receives a power on/off flag 149 and a suspend/resume flag 150 from the register 148 and outputs the logical add value of the power on/off flag 149 and the suspend/resume flag 150 from the register 148.

The switch 147 is connected to the input power source Vin and a voltage source of the display device 151. The switch 147 controls supply of the input voltage Vin to the voltage source of the

display device 151 according to the power on/off flag 149 in the register 148.

The voltage source of the display device 151 converts the input power source Vin, which is supplied through the switch 147, into a voltage for the display device 113 and supplies the voltage to the display device 113.

The register 148 is connected to the CPU 101. Values are written in the power on/off flag 149 and the suspend/resume flag 150 in the register 148 in response to commands from the CPU 101.

The CPU 101 detects the type of the data of the file with the method described later and writes the values to the power on/off flag 149 and the suspend/resume flag 150 in the register 148 according to the type of the data of the file.

The graphics board controller 114 turns the switch 147 on when the power on/off flag 149 in the register 148 is "1"(one). If the switch 147 turns on, the input power source Vin is supplied to the voltage source of the display device 151. Then, the voltage source of the display device 151 supplies power to the display device 113, so that the display device 113 can display pictures.

When the power on/off flag 149 in the register 148 is "1"(one), the gate 145 turns on, so that the graphics board 112 is connected to both the voltage source 130 and the bus 115. The graphics board 112 drives the display device 113 to display the pictures on the display device 113 according to the display data from the bus 115.

The switch 147 turns off if the power on/off flag 149 in the register 148 is "0"(zero). If the switch 147 turns off, the input power source Vin does not supply the power to the voltage source of the display device 151, so that the power for the display device 113 is not generated and the display

device 113 turns off.

If the power on/off flag 149 in the register 148 is "0"(zero), the gate 145 turns off, so that the graphics board 112 is disconnected from both the voltage source 130 and the bus 115. As a result, the graphics board 112 stops.

The graphics controller 114 turns the gate 145 on when the suspend/resume flag 150 in the register 148 is "1"(one). If the gate 145 turns on, the graphics board 112 is connected to both the voltage source 130 and the bus 115. Therefore, the graphics board becomes operational. The graphics board 112 drives the display device 113 to display the pictures on the display device 113 according to the display data from the bus 115.

If the suspend/resume flag 150 in the register 148 is "0"(zero), the gate 145 turns off, so that the graphics board 112 is disconnected from the voltage source 130 and the bus 115. Therefore, the graphics board 112 stops.

Next, the operation of the CPU 101 will be explained. Fig.6 shows a flowchart to register a power save mode according to the first embodiment of the present invention. At the first step S1-1, a procedure to register the power save mode is selected in the CPU 101. Then, at the second step S1-2, types of data are defined. Next, for each predefined type of data, information on devices in which to shut the power down or to enter into the suspend mode when the predefined type of data is detected is registered. The information which is to be registered include names of the devices, the type of power save mode, such as power on/off or suspend/resume, and so on.

Next, the registered information in the step S1-2 is written in a power save mode table. The power save mode table is assigned in the memory

102.

Fig.7 shows the data structure of the power save mode table according to the first embodiment of the present invention. The names of the devices and their power save information, which shows what kind of power save control is to be performed, such as power on/off or suspend/resume, in each type of data such as MPEG, MIDI and so on, are registered in the power save mode table.

The CPU 101 detects the type of data and determines the kind of power save control to be done by referring to the power save mode table. Then, the CPU 101 executes the power save control by controlling each of the board controllers according to the determined power save control mode described above.

Fig.8 shows a flowchart of the power save control in the CPU 101 according to the first embodiment of the present invention.

The CPU 101 reads data from the CD-ROM 122 which is inserted in the CD-ROM drive 108 according to the desired application program. At the same time, the CPU 101 executes the power save control in parallel with the execution of the application program.

The CPU 101 starts the execution of the power save control when the data is read from the CD-ROM 122 according to the application program (S2-1). Next, the CPU 101 detects the type of the data (S2-2). Then, the CPU 101 reads the power save information from the predetermined power save mode table according to the type of the data detected in step S2-2, the power save information including such as the names of the devices and the power save mode to be applied to the devices, i.e., the power on/off mode or the suspend/resume mode (S2-3).

The power save information which is read

in step S2-3 is written to each of the registers 127, 136, 142, 148 in each of the board controllers 105, 107, 111, 114 according to the names of the devices which are also read from the power save mode table. Each of the board controllers 105, 107, 111, 114 executes the power save control, such as the power on/off mode or the suspend/resume mode, based on the power save information stored in each of the registers 127, 136, 142, 148 (S2-4).

Steps from S2-1 to S2-4 described above are repeated until the CPU 101 halts the execution of the application program when the end of the application program is detected.

It is possible that users can freely select the boards for which the power save control will be applied by writing the information in the power save mode table shown in Fig.7 according to the types of the data with the procedure shown in Fig.6.

It is possible to collect all the separate registers 127, 136, 142, 148, which are associated with each of the board controllers 105, 107, 111, 114 in the first embodiment, into one register.

Fig. 9 is another example of the data structure of the register for the power save mode table according to the first embodiment of the present invention. Fig.9(A) shows the construction of the register and Fig.9(B) shows the data structure of the power save information in each element of the register.

A register 160 has of memory areas from 161-1 to 161-n which store the power save information for each device. Each of the memory areas 161-1 to 161-n stores the device name or identification number information 162a and the power save information 162b applied to the corresponding device. Each of the board controllers 105, 107, 111,

114 is controlled during its power save operation with the corresponding power save information held in the register 160.

In this embodiment, the power save control is executed according to the power save mode table. However, the power save control may be executed according to predetermined power save information associated with the data which is used in the application program.

Fig.10 shows a flowchart of the power save control in the CPU according to a second embodiment of the present invention. Explanation of the structure is omitted because it is the same structure as shown in Fig.1 to Fig.6.

The CPU 101 reads the data from the CD-ROM 122 which is inserted in the CD-ROM drive 108 according to the application program. At the same time, the CPU 101 executes the power save control in parallel with the execution of the application program.

The CPU 101 starts the execution of the power save control when the data is read from the CD-ROM 122 according to the application program (S3-1). Next, the CPU 101 detects the power save information prerecorded on the CD-ROM 122 just before the data which is used in the application program (S3-2).

The power save information prerecorded just before the data is explained below.

Fig.11 shows the structure of the data processed by the CPU according to the second embodiment of the present invention. Fig.11(A) shows the structure of the data 170 which is recorded in the CD-ROM 122 and Fig.11(B) shows the structure of the power save information 172. In this embodiment, the power save information 172 is prerecorded just before the main data 171 in the

data 170. The power save information 172 shows the devices which do not use the main data 171.

The power save information 172 includes a flag 173, information to designate the devices 174 and the power save control information 175. If the flag 173 is off, the power save control is executed for the devices which are designated by the information to designate the devices 174 according to the power save control information 175. On the other hand, if the flag 173 is on, the power save control is executed for other devices which are not designated by the information to designate the devices 174 according to the power save control information 175. Thus, the information to designate the devices 174 designates the devices to execute the power save control according to the power save control information 175 when the flag 173 is off. The power save control information 175 shows the kinds of the power save control operations which are to be executed, the kinds includes such as the power on/off control or the suspend/resume control.

Next, the explanation of the flowchart of Fig.10 will be continued.

When the power save information 172 is detected in step S3-2, the CPU 101 writes the power save control information 175 in each of the registers 127, 136, 142, 148 in each of the board controllers 105, 107, 111, 114 according to the information to designate the devices 174 (S3-3). Then, each of the board controllers 105, 107, 111, 114 executes the power save operation according to the power save control information 175 written in each of the registers 127, 136, 142, 148 (S3-4).

Step from S3-1 to S3-4 described above are repeated until the CPU 101 halts the execution of the application program when the end of the application program is detected.

This embodiment enables automatic execution of the power save control for each board according to the power save information recorded on the recording media.

The present invention is not limited to the specifically disclosed embodiments, and variations and modifications may be made without departing from the scope of the present invention.

The present application is based on Japanese priority application No.10-192009 filed on July 7, 1998, the entire contents of which are thereby incorporated by reference.

WHAT IS CLAIMED IS:

1. An information processing apparatus which drives a plurality of driving means according to data to be processed, the information processing apparatus comprising:

a detection unit which detects type of the data to be processed; and

a control unit which controls each of said plurality of driving means according to said type of the data to be processed.

2. The information processing apparatus as claimed in claim 1, wherein said control unit controls a power source which supplies power to said plurality of driving means.

3. The information processing apparatus as claimed in claim 2, wherein said control unit supplies power to each of said plurality of driving means that can process said data to be processed and stops supplying power to each of said plurality of driving means that cannot process said data to be processed.

4. An information processing apparatus which drives a plurality of driving means according to data to be processed, the information processing apparatus comprising:

a control unit which controls each of said plurality of driving means according to control data added to said data to be processed.

5. The information processing apparatus as claimed in claim 4, wherein said control unit controls a power source which supplies power to said plurality of driving means.

6. A power control method which controls power supplied to a plurality of driving means to be supplied with data to be processed, the power control method comprising the steps of:

(a) detecting a type of the data to be processed; and

(b) controlling each of said plurality of driving means according to said type of the data to be processed.

7. The power control method as claimed in claim 6, wherein said step (b) controls a power source which supplies the power to said plurality of driving means.

8. The power control method as claimed in claim 7, wherein said step (b) supplies power to each of said plurality of driving means that can process said data to be processed, and stops supplying power to each of said plurality of driving means that cannot process said data to be processed.

9. A power control method which controls power supplied to a plurality of driving means to be supplied with data to be processed, the power control method comprising:

a step of controlling each of said plurality of driving means according to control data added to said data to be processed.

10. The power control method as claimed in claim 9, wherein said step controls a power source which supplies the power to said plurality of driving means.

11. A computer readable recording medium from which a program can be read by a computer which drives a plurality of driving means according to data to be processed, the computer readable recording medium comprising:

the program comprising:

a detection procedure for detecting a type of the data to be processed; and

a control procedure for controlling each of said plurality of driving means according to said type of the data to be processed.

12. The computer readable recording medium as claimed in claim 11, wherein said control procedure controls a power source which supplies power to said plurality of driving means.

13. The computer readable recording medium as claimed in claim 11, wherein said control procedure supplies power to each of said plurality of driving means that can process said data to be processed and stops supplying the power to each of said plurality of driving means which can not process said data to be processed.

14. A computer readable recording medium from which a program can be read by a computer which drives a plurality of driving means according to data to be processed, the computer readable recording medium comprising:

the program comprising:

a control procedure for controlling each of said plurality of driving means according to

control data added to said data to be processed.

15. The computer readable recording medium as claimed in claim 14, wherein said control procedure controls a power source which supplies power to said plurality of driving means.

16. The computer readable recording medium as claimed in claim 14, wherein said control procedure supplies power to each of said plurality of driving means that can process said data to be processed and stops supplying the power to each of said plurality of driving means which can not process said data to be processed.

17.A computer readable recording medium comprising:

data comprising:

driving data to be supplied to driving means; and

control data used to control other driving means.

18. The computer readable recording medium as claimed in claim 16, wherein said control data is

recorded just before said driving data.

5

ABSTRACT OF THE DISCLOSURE

An information processing apparatus which drives a plurality of driving units according to data to be processed includes a first unit which detects a type of the data to be processed and a second unit which controls each of the plurality of driving units according to the type of the data to be processed. Power save control information and names of devices applied to the power save control are read from a predetermined power save mode table according to the detected type of the data and a power save operation is executed for the driving units according to the power save control information.

FIG. 1

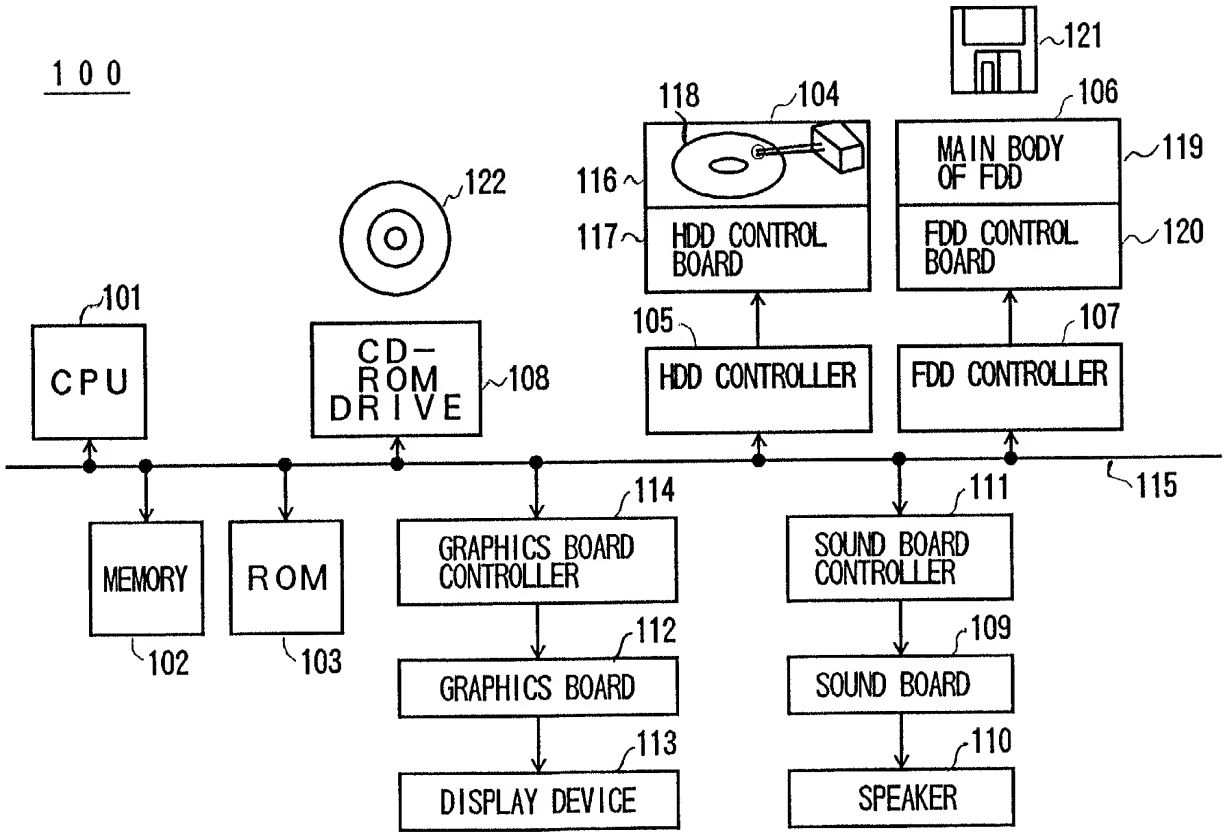

100
121
118
104
106
MAIN BODY OF FDD
119
116
122
HDD CONTROL BOARD
117
FDD CONTROL BOARD
120
101
105
107
CPU
CD-ROM DRIVE
108
HDD CONTROLLER
FDD CONTROLLER
115
114
111
MEMORY
ROM
GRAPHICS BOARD CONTROLLER
SOUND BOARD CONTROLLER
102
103
112
109
GRAPHICS BOARD
SOUND BOARD
113
110
DISPLAY DEVICE
SPEAKER

FIG. 2

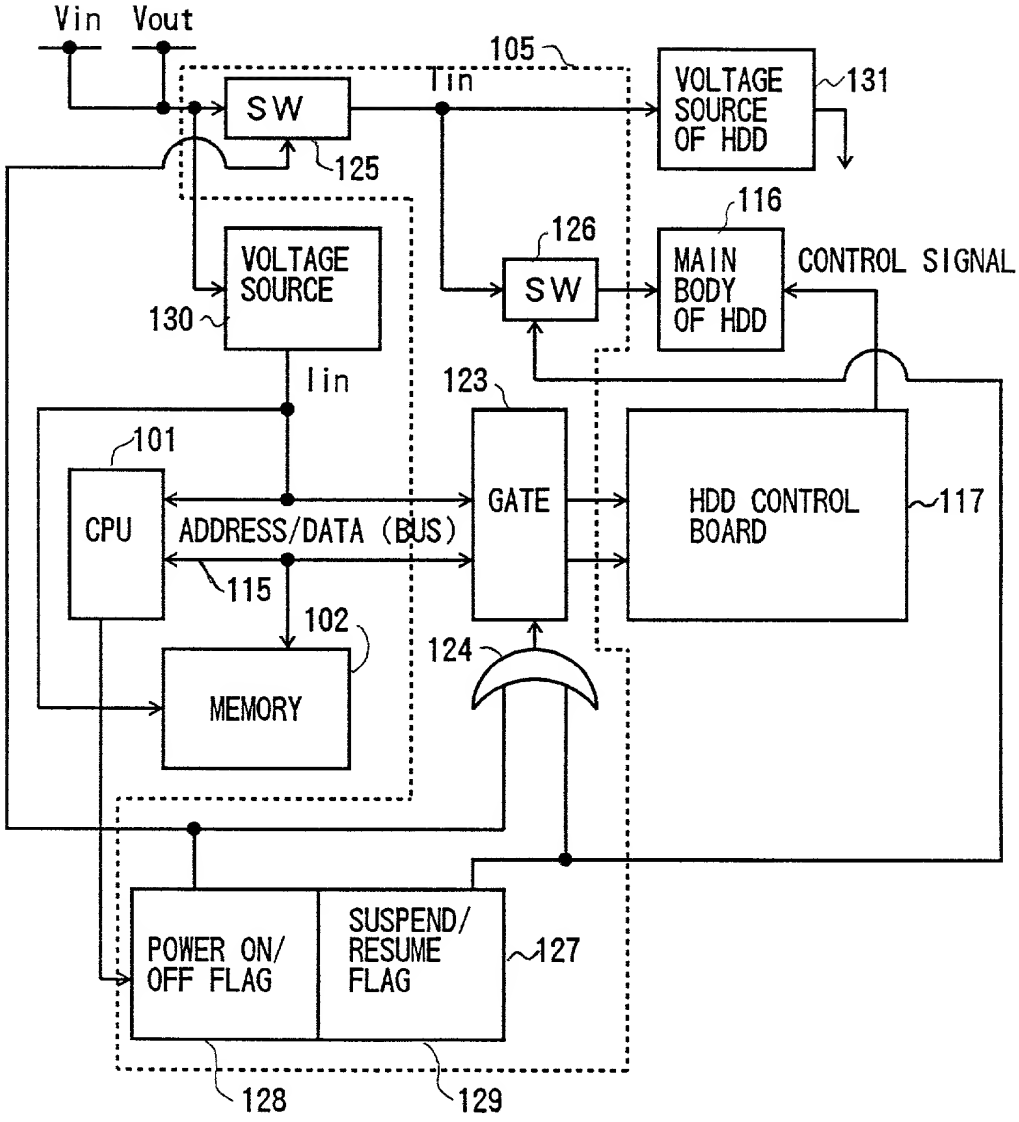

Vin
Vout
105
Iin
SW
125
VOLTAGE SOURCE OF HDD
131
116
126
VOLTAGE SOURCE
130
SW
MAIN BODY OF HDD
CONTROL SIGNAL
Iin
123
101
CPU
ADDRESS/DATA (BUS)
GATE
HDD CONTROL BOARD
117
115
102
124
MEMORY
POWER ON/ OFF FLAG
SUSPEND/ RESUME FLAG
127
128
129

FIG. 3

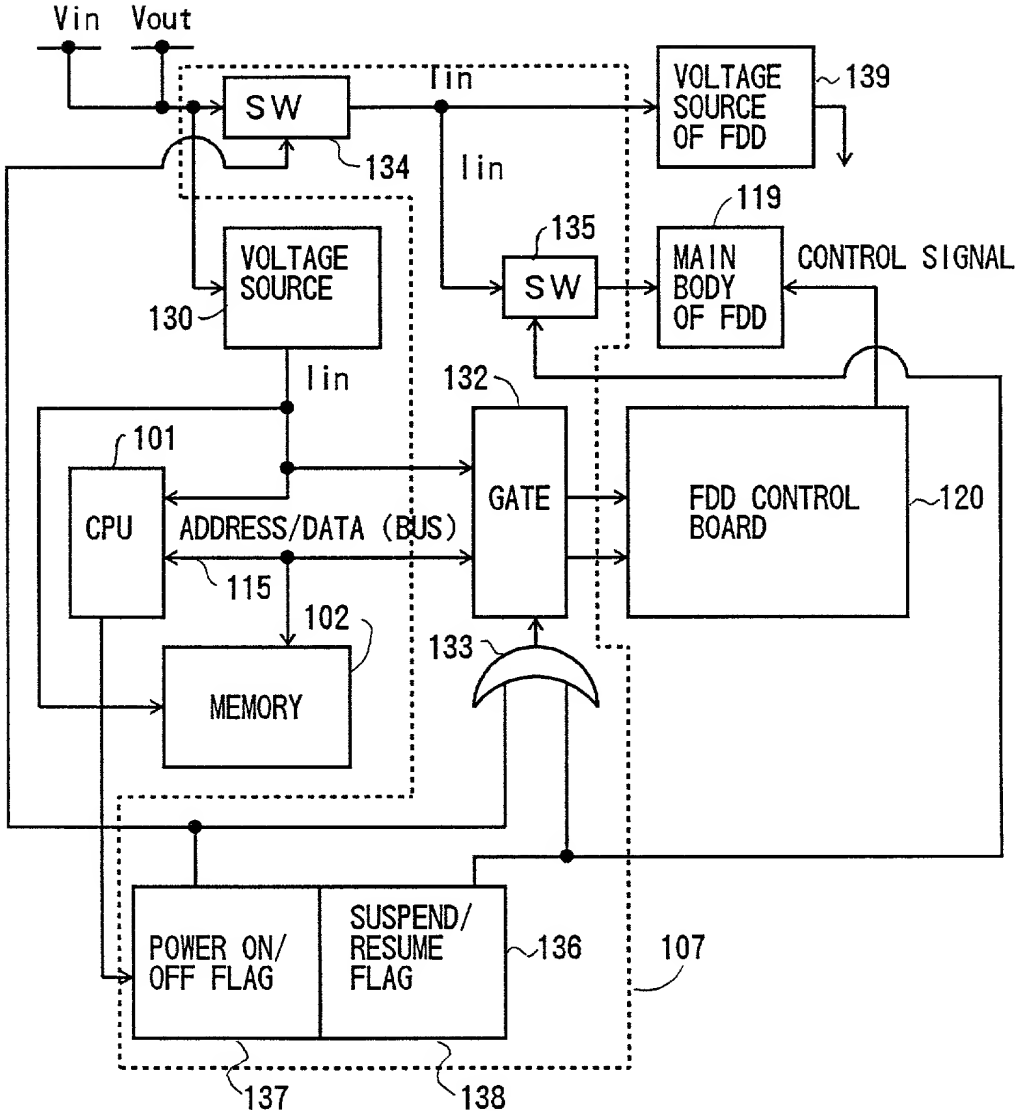

Vin
Vout
SW
134
Iin
Iin
VOLTAGE SOURCE OF FDD
139
119
135
SW
MAIN BODY OF FDD
CONTROL SIGNAL
VOLTAGE SOURCE
130
Iin
132
101
CPU
ADDRESS/DATA (BUS)
115
GATE
FDD CONTROL BOARD
120
102
133
MEMORY
POWER ON/ OFF FLAG
SUSPEND/ RESUME FLAG
136
107
137
138

FIG. 4

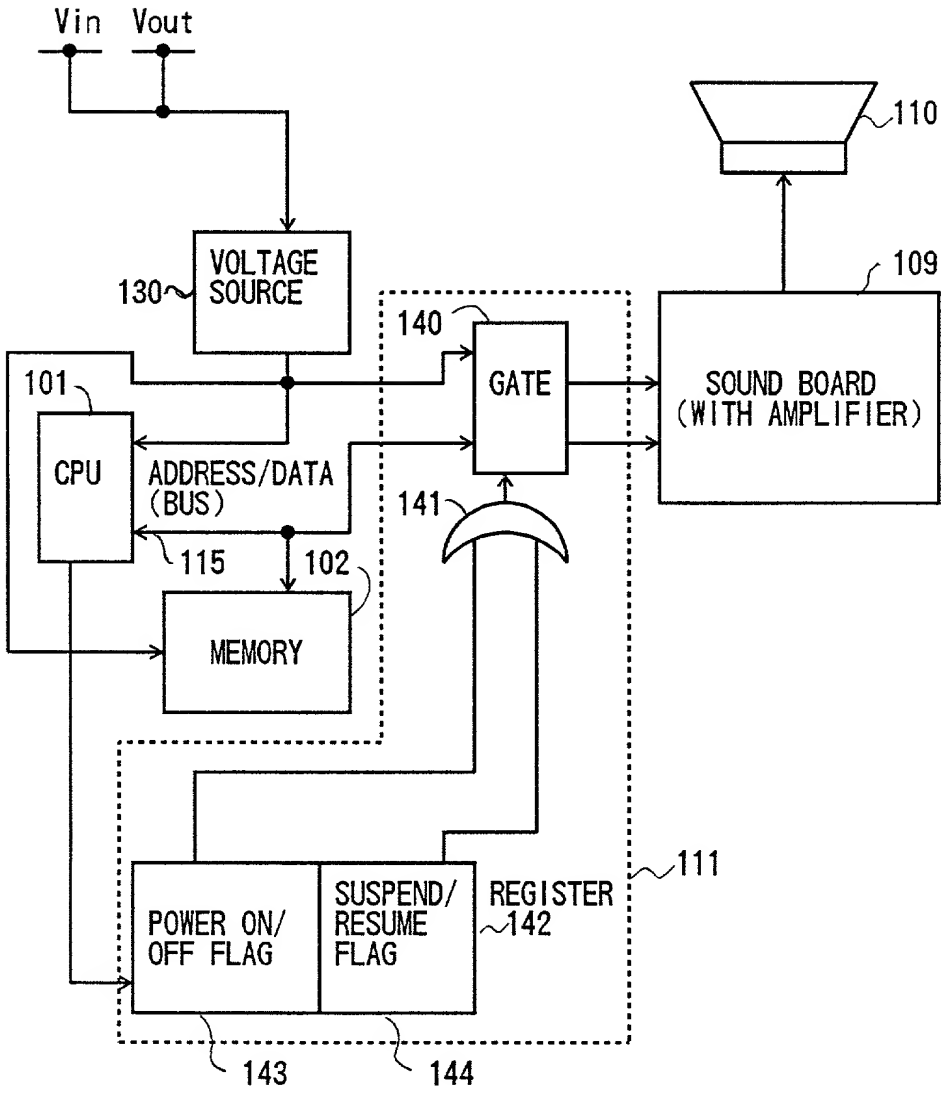

Vin
Vout
110
VOLTAGE SOURCE
130
109
140
GATE
SOUND BOARD (WITH AMPLIFIER)
101
CPU
ADDRESS/DATA (BUS)
141
115
102
MEMORY
111
POWER ON/ OFF FLAG
SUSPEND/ RESUME FLAG
REGISTER
142
143
144

FIG. 5

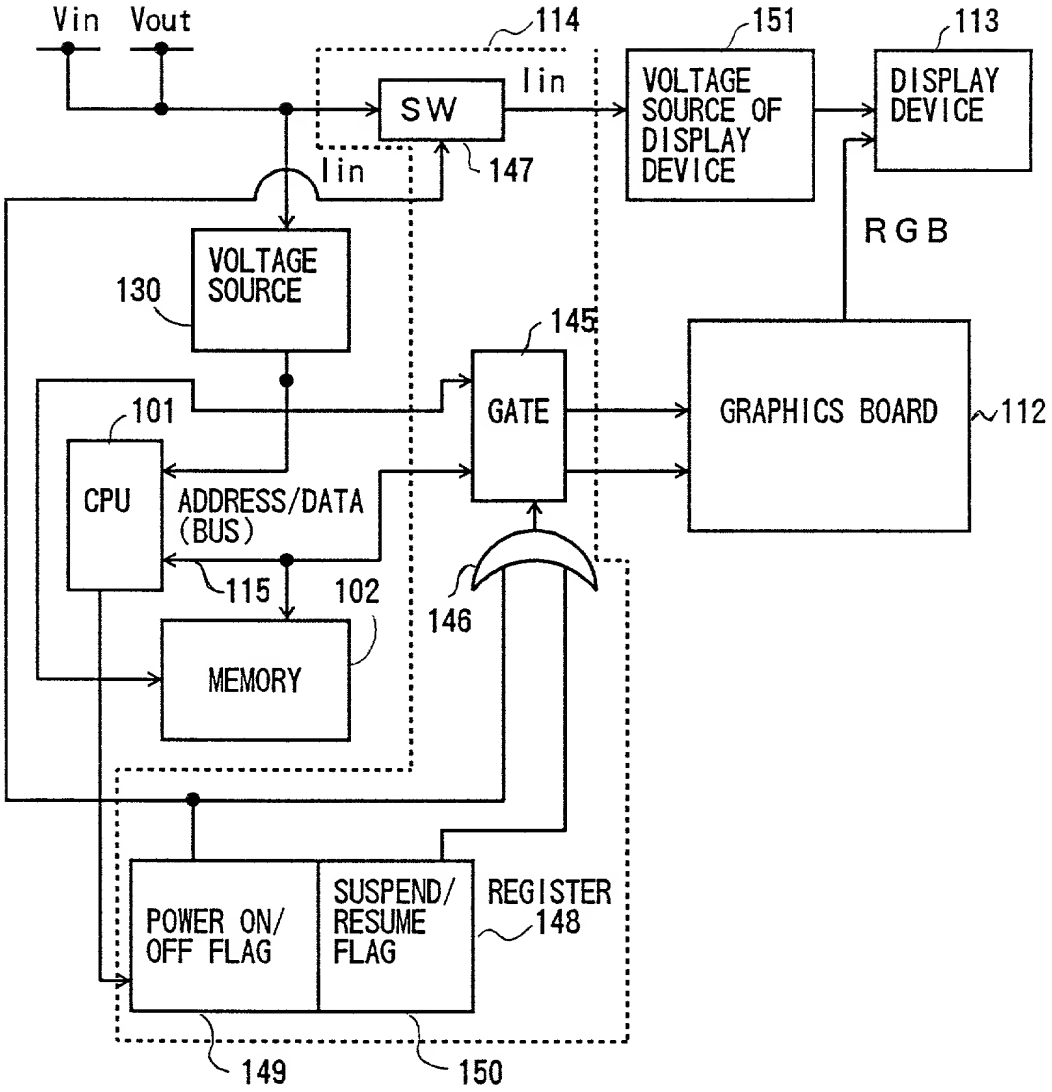

Vin
Vout
114
151
113
SW
Iin
VOLTAGE SOURCE OF DISPLAY DEVICE
DISPLAY DEVICE
Iin
147
RGB
VOLTAGE SOURCE
130
145
GATE
GRAPHICS BOARD
112
101
CPU
ADDRESS/DATA (BUS)
115
102
146
MEMORY
POWER ON/ OFF FLAG
SUSPEND/ RESUME FLAG
REGISTER
148
149
150

FIG. 6

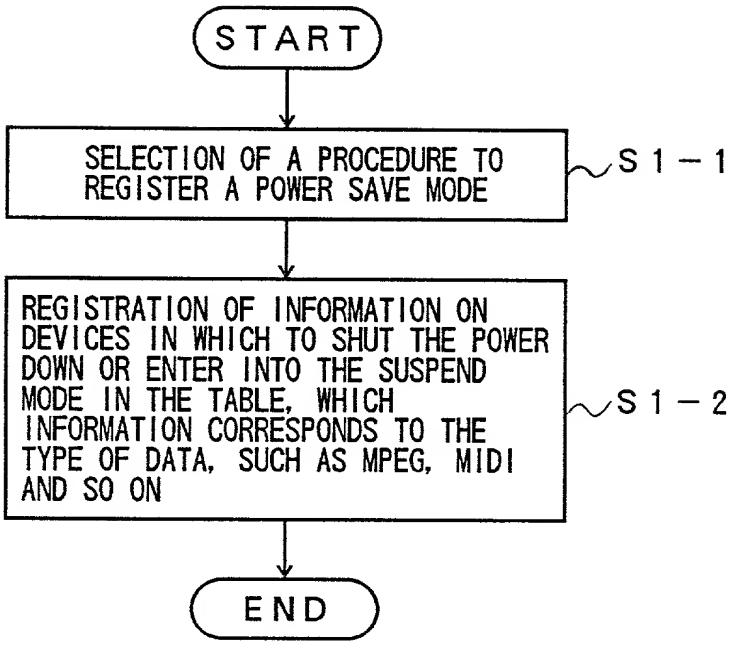


FIG. 7

MPEG	DEVICE 1-1	SUSPEND	・・・・	DEVICE 1-n	POWER OFF
MIDI	DEVICE 2-1	POWER OFF	・・・・	DEVICE 2-n	SUSPEND
・・・・	・・・・・	・・・・・	・・・・	・・・・・	・・・・・

FIG. 8

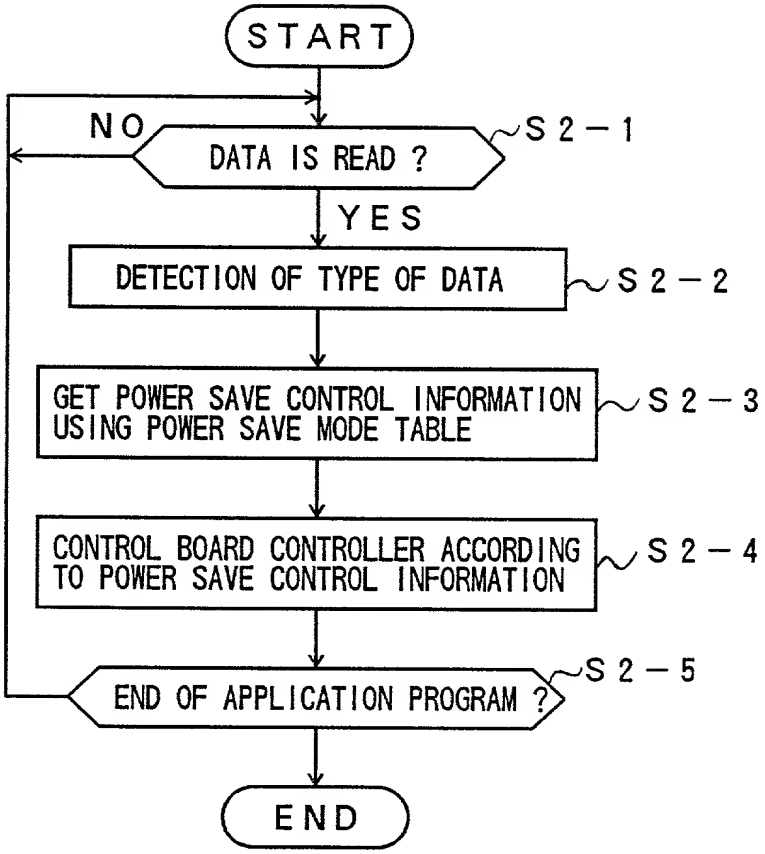

START
NO
DATA IS READ ?
S 2 – 1
YES
DETECTION OF TYPE OF DATA
S 2 – 2
GET POWER SAVE CONTROL INFORMATION USING POWER SAVE MODE TABLE
S 2 – 3
CONTROL BOARD CONTROLLER ACCORDING TO POWER SAVE CONTROL INFORMATION
S 2 – 4
END OF APPLICATION PROGRAM ?
S 2 – 5
END

FIG. 9

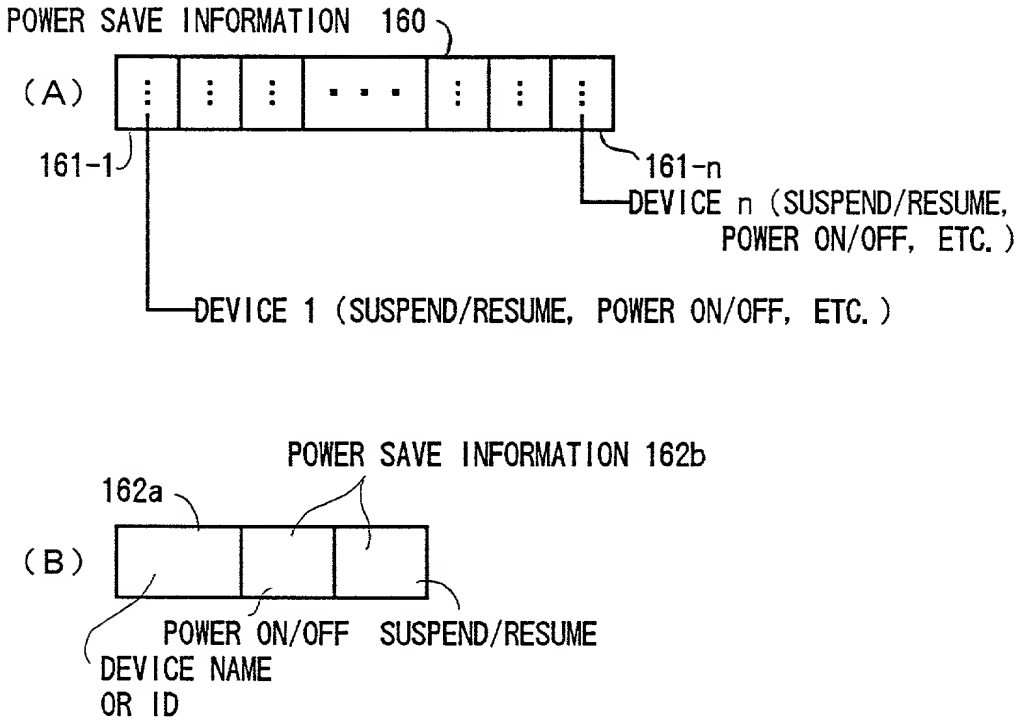

POWER SAVE INFORMATION 160
(A)
161-1
161-n
DEVICE n (SUSPEND/RESUME, POWER ON/OFF, ETC.)
DEVICE 1 (SUSPEND/RESUME, POWER ON/OFF, ETC.)
POWER SAVE INFORMATION 162b
162a
(B)
POWER ON/OFF
SUSPEND/RESUME
DEVICE NAME OR ID

FIG. 10

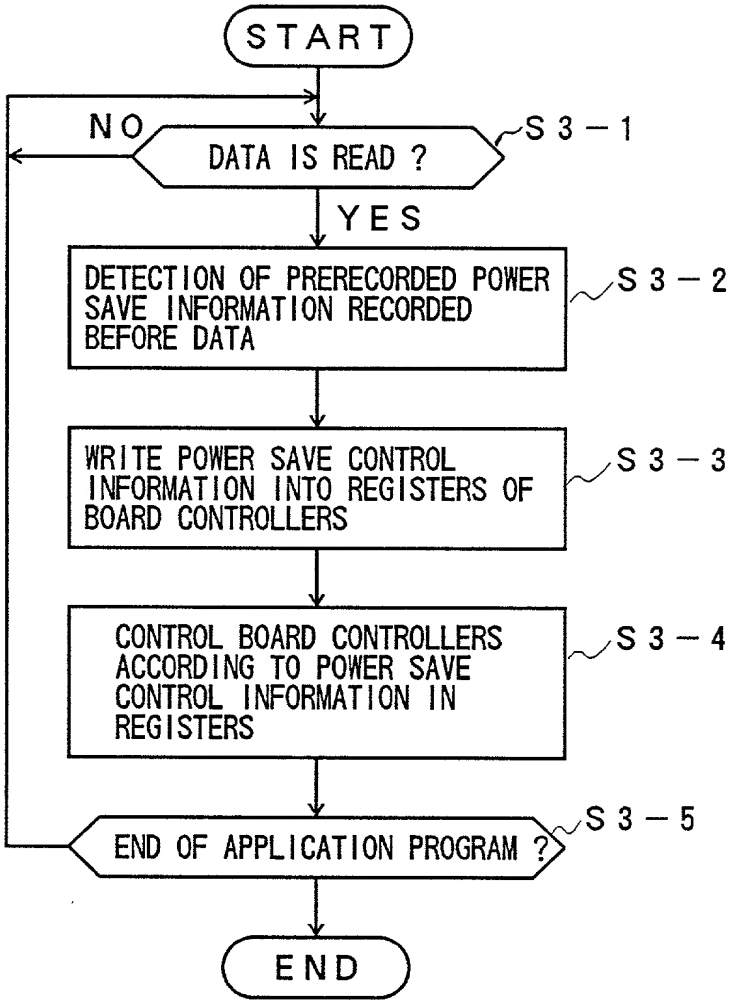
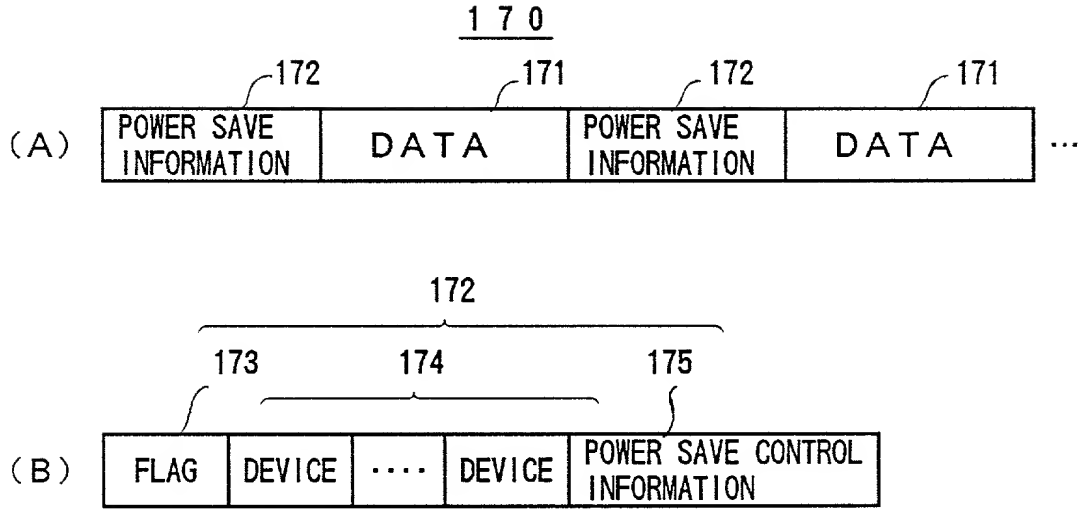

START
NO
DATA IS READ ?
S 3 − 1
YES
DETECTION OF PRERECORDED POWER SAVE INFORMATION RECORDED BEFORE DATA
S 3 − 2
WRITE POWER SAVE CONTROL INFORMATION INTO REGISTERS OF BOARD CONTROLLERS
S 3 − 3
CONTROL BOARD CONTROLLERS ACCORDING TO POWER SAVE CONTROL INFORMATION IN REGISTERS
S 3 − 4
END OF APPLICATION PROGRAM ?
S 3 − 5
END

FIG. 11


170
172
171
172
171
(A)
POWER SAVE INFORMATION
DATA
POWER SAVE INFORMATION
DATA
...
172
173
174
175
(B)
FLAG
DEVICE
....
DEVICE
POWER SAVE CONTROL INFORMATION

PTO/SB/106 (8-96)
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Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

INFORMATION PROCESSING APPARATUS, POWER CONTROL METHOD AND RECORDING MEDIUM

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ _月_日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____に訂正されました。

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条(a)-(d)項又は３６５条(b)項に基き下記の、米国以外の国の少なくとも一ヶ国を指定している特許協力条約３６５(a)項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、欄内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) (Patent Application)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
No.10-192009	Japan	7/July/1998	☐
			☐

私は、第３５編米国法典１１９条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(c)に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は与に許可された特許の有効性が失われることを認識し、よってここに下記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

James D. Halsey, Jr., 22,729; Harry John Staas, 22,010; David M. Pitcher, 25,908; John C. Garvey, 28,607; J. Randall Beckers, 30,358; William F. Herbert, 31,024; Richard A. Gollhofer, 31,106; Mark J. Henry, 36,162; Gene M. Garner II, 34,172; Michael D. Stein, 37,240; Paul I. Kravetz, 35,230; Gerald P. Joyce, III, 37,648; Todd E. Marlette, 35,269; Harlan B. Williams, Jr., 34,756; George N. Stevens, 36,938; Michael C. Soldner, P-41,455 and William M. Schertler, 35,348 (agent)

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Direct Telephone Calls to: *(name and telephone number)*

STAAS & HALSEY
(202) 434-1500

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発明者の署名 日付	Inventor's signature Date Yoshifusa Togawa March 25, 1999
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国籍	Citizenship Japan
私書箱	Post Office Address c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211-8588 Japan
第二共同発明者	Full name of second joint inventor, if any
第二共同発明者 日付	Second inventor's signature Date
住所	Residence
国籍	Citizenship
私書箱	Post Office Address

（第三以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)